ing, physical layout analysis and testing of masks or semiconductor devices, having either of the following:

a. Target-to-beam position feedback control precision of 0.25 micrometre or finer; or

b. Digital-to-analogue conversion resolution exceeding 12 bit;

1032. 6. "Stored programme controlled" automatic loading multi-chamber central wafer handling systems, having interfaces for wafer input and output, to which more than two pieces of semiconductor processing equipment are to be connected, to form an integrated system in a vacuum environment for sequential multiple wafer processing;

NOTE:

1032.6. does not embargo automatic robotic wafer handling systems not designed to operate in a vacuum environment.

1032. 7. "Stored programme controlled" lithography equipment, as follows:

1032. 7. a. Align and expose step and repeat equipment for wafer processing using photo-optical or X-ray methods, having any of the following:

1. A light source wavelength shorter than 400 nm;
2. A numerical aperture more than 0.40; or
3. An overlay accuracy of ± 0.20 micrometre (3 sigma) or better;

NOTE:

1032.7.a. does not embargo align and expose step and repeat equipment having all of the following:

1. A light source wavelength of 436 nm or more;
2. A numerical aperture 0.38 or less; and
3. An image size diameter 22 mm or less.

1032. 7. b. Equipment specially designed for mask making or semiconductor device processing using deflected focussed electron beam, ion beam or "laser" beam, with any of the following:

1. A spot size smaller than 0.2 micrometre;
2. Capable of producing a pattern with a feature size of less than 1 micrometre; or
3. An overlay accuracy of better than ± 0.20 micrometre (3 sigma);

1032. 8. Masks or reticles, as follows:

a. For integrated circuits embargoed by 1031.1.;

b. Multi-layer masks with a phase shift layer;

1032. 9. "Stored programme controlled" test equipment, specially designed for testing semiconductor devices and un-encapsulated dice, as follows:

1032. 9. a. For testing S-parameters of transistor devices at frequencies exceeding 31 GHz;

1032. 9. b. For testing integrated circuits, and "assemblies" thereof, and capable of performing functional (truth table) testing at a pattern rate of more than 40 MHz;

NOTE:

1032.9.b. does not embargo test equipment specially designed for testing:

1. "Assemblies" or a class of "assemblies" for home or entertainment applications;
2. Unembargoed electronic components, "assemblies" or integrated circuits.

1032. 9. c. For testing microwave integrated circuits at frequencies exceeding 3 GHz;

NOTE:

1032.9.c. does not embargo test equipment specially designed for testing microwave integrated circuits for equipment designed or rated to operate in the Standard Civil Telecommunication Bands at frequencies not exceeding 31 GHz.

1032. 9. d. Electron beam systems designed for operation at or below 3 keV, or "laser" beam systems, for the non-contactive probing of powered-up semiconductor devices, with both of the following:

1. Stroboscopic capability with either beam-blanking or detector strobing; and
2. An electron spectrometer for voltage measurement with a resolution of less than 0.5 V.

NOTE:

1032.9.d. does not embargo scanning electron microscopes, except when specially designed and instrumented for the non-contactive probing of powered-up semiconductor devices.

1033. MATERIALS

1033. 1. Hetero-epitaxial materials consisting of a "substrate" with stacked epitaxially grown multiple layers of:

a. Silicon;

b. Germanium; or

c. III/V compounds of gallium or indium;

Technical Note:

III/V compounds are polycrystalline or binary or complex monocrystalline products consisting of elements of groups IIIA and VA of Mendeleyev's periodic classification table (gallium arsenide, gallium-aluminium arsenide, indium phosphide, etc.).

1033. 2. Resist materials, as follows, and "substrates" coated with embargoed resists:

a. Positive resists with a spectral response optimized for use below 370 nm;

b. All resists, for use with electron beams or ion beams, with a sensitivity of 0.01 microcoulomb/mm^2 or better;

c. All resists, for use with X-rays, with a sensitivity of 2.5 mJ/mm^2 or better;

d. All resists optimized for surface imaging technologies, including silyated resists;

Technical Note:

Silyation techniques are defined as processes incorporating oxidation of the resist surface to enhance performance for both wet and dry developing.

1033. 3. Metal-organic compounds of aluminium, gallium or indium, having a purity (metal basis) better than 99.999%;

1033. 4. Hydrides of phosphorus, arsenic or antimony, having a purity better than 99.999%, even diluted in neutral gases.

NOTE:

1033.4. does not embargo hydrides containing 20% molar or more of rare gases or hydrogen.

1034. SOFTWARE

1034. 1. "Software" specially designed for the "development" or "production" of equipment embargoed by 1031.1.b. to 1031.2.h. or 1032.;

1034. 2. "Software" specially designed for the "use" of "stored programme controlled" equipment embargoed by 1032.;

1034. 3. Computer-aided-design (CAD) "software" for semiconductor devices or integrated circuits, having any of the following:

a. Design rules or circuit verification rules;

b. Simulation of the physically laid out circuits; or

c. Lithographic processing simulators for design.

Technical Note:

A lithographic processing simulator is a "software" package used in the design phase to define the sequence of lithographic, etching and deposition steps for translating masking patterns into specific topographical patterns in conductors, dielectrics or semiconductor material.

NOTE:

1034.3. does not embargo "software" specially designed for schematic entry, logic simulation, placing and routing, layout verification or pattern generation tape;

N.B.:

Libraries, design attributes or associated data for the design of semiconductor devices or integrated circuits are considered as technology.

1035. TECHNOLOGY

1035. 1. Technology according to the General Technology Note for the "development" or "production" of equipment or materials embargoed by 1031, 1032 or 1033;

NOTE:

1035.1. does not embargo technology for the "development" or "production" of:

a. Microwave transistors operating at frequencies below 31 GHz;

b. Integrated circuits embargoed by 1031.1.a.3. to 11., having both of the following characteristics:

1. Using technology of one micrometre or more, and
2. Not incorporating multi-layer structures.

N.B.:

This Note does not preclude the export of multilayer technology for devices incorporating a maximum of two metal layers and two polysilicon layers.