1045. cont'd.

***Step 2:* TP for each supported operand length WL:**

Adjust the effective rate R (or R') by the word length adjustment L as follows:

$TP = R \times L$, where $L = (1/3 + WL/96)$

Note:

The word length WL used in these calculations is the operand length in bits. (If an operation uses operands of different lengths, select the largest word length.)

The combination of a mantissa ALU and an exponent ALU of a floating point processor or unit is considered to be one "CE" with a Word Length (WL) equal to the number of bits in the data representation (typically 32 or 64) for purposes of the "CTP" calculation. This adjustment is not applied to specialized logic processors which do not use XOR instructions. In this case TP = R.

Select the maximum resulting value of TP for:

Each XP-only "CE" (R_{xp});

Each FP-only "CE" (R_{fp});

Each combined FP and XP "CE" (R);

Each simple logic processor not implementing any of the specified arithmetic operations; ***and***

Each special logic processor not using any of the specified arithmetic or logic operations.

***Step 3:* "CTP" for aggregations of "CEs", including CPUs.**

For a CPU with a single "CE",

"CTP" = TP

(for "CEs" performing both fixed and floating point operations

$TP = \max (TP_{fp}, TP_{xp})$)

"CTP" for aggregations of multiple "CEs" operating simultaneously is calculated as follows:

Notes:

1. *For aggregations that do not allow all of the "CEs" to run simultaneously, the possible combination of "CEs" that provides the largest "CTP" should be used. The TP of each contributing "CE" is to be calculated at its maximum value theoretically possible before the "CTP" of the combination is derived.*

   N.B.:

   To determine the possible combinations of simultaneously operating "CEs", generate an instruction sequence that initiates operations in multiple "CEs", beginning with the slowest "CE" (the one needing the largest number of cycles to complete its operation) and ending with the fastest "CE". At each cycle of the sequence, the combination of "CEs" that are in operation during that cycle is a possible combination. The instruction sequence must take into account all hardware and/or architectural constraints on overlapping operations.
2. *A single integrated circuit chip or board assembly may contain multiple "CEs".*
3. *Simultaneous operations are assumed to exist when the computer manufacturer claims concurrent, parallel or simultaneous operation or execution in a manual or brochure for the computer.*
4. *"CTP" values are not to be aggregated for "CE" combinations (inter)connected by "Local Area Networks", Wide Area Networks, I/O shared connections/devices, I/O controllers and any communication interconnection implemented by software.*
5. *"CTP" values must be aggregated for multiple "CEs" specially designed to enhance performance by aggregation, operating simultaneously and sharing memory,- or multiple memory/"CE"- combinations operating simultaneously utilising specially designed hardware.*

This aggregation does not apply to "assemblies" described by 1041.3.d.

"CTP" = $TP_1 + C_2 \times TP_2 + \ldots + C_n \times TP_n$,

where the TPs are ordered by value, with TP_1 being the highest, TP_2 being the second highest, ..., and TP_n being the lowest. C_i is a coefficient determined by the strength of the interconnection between "CEs", as follows:

For multiple "CEs" operating simultaneously and sharing memory:

$C_2 = C_3 = C_4 = \ldots = C_n = 0.75$

Notes:

1. When the "CTP" calculated by the above method does not exceed 194 Mtops, the following formula may be used to calculate C_i:

$$C_i = \frac{0.75}{\sqrt{m}} \qquad (i = 2, \ldots, n)$$

where m = the number of "CEs" or groups of "CEs" sharing access.

provided:

a. *The TP_i of each "CE" or group of "CEs" does not exceed 30 Mtops;*

b. *The "CEs" or groups of "CEs" share access to main memory (excluding cache memory) over a single channel;* ***and***

c. *Only one "CE" or group of "CEs" can have use of the channel at any given time.*

N.B.:

This does not apply to items controlled under Category 1030.

2. *"CEs" share memory if they access a common segment of solid state memory. This memory may include cache memory, main memory or other internal memory. Peripheral memory devices such as disk drives, tape drives or RAM disks are not included.*

For Multiple "CEs" or groups of "CEs" not sharing memory, interconnected by one or more data channels:

$C_i = 0.75 \times k_i \quad (i = 2, \ldots, 32)$ *(see Note below)*

$= 0.60 \times k_i \quad (i = 33, \ldots, 64)$

$= 0.45 \times k_i \quad (i = 65, \ldots, 256)$

$= 0.30 \times k_i \quad (i > 256)$

The value of C_i is based on the number of "CE"s, not the number of nodes.

where k_i = *min (S/K_r, 1), and*

K_r = *normalizing factor of 20 MByte/s.*

S_i = *sum of the maximum data rates (in units of MByte/s) for all data channels connected to the i^{th} "CE" or group of "CEs" sharing memory.*

When calculating a C_i for a group of "CEs", the number of the first "CE" in a group determines the proper limit for C_i. For example, in an aggregation of groups consisting of 3 "CEs" each, the 22nd group will contain "CE"$_{64}$, "CE"$_{65}$ and "CE"$_{66}$ The proper limit for C_i for this group is 0.60.

Aggregation (of "CEs" or groups of "CEs") should be from the fastest-to-slowest; i.e.: $TP_1 \geq TP_2 \geq \ldots \geq TP_n$, and in the case of $TP_i = TP_{i+1}$, from the largest to smallest; i.e.: $C_i \geq C_{i+1}$

Note:

The k_i factor is not to be applied to "CEs" 2 to 12 if the TP_i of the "CE" or group of "CEs" is more than 50 Mtops; i.e. C_i for "CEs" 2 to 12 is 0.75.

1050. Telecommunications

Notes:

1. *The embargo status of components, "lasers", test and production equipment, materials and "software" therefor which are specially designed for telecommunications equipment or systems is defined in this Category.*
2. *"Digital computers", related equipment or "software", when essential for the operation and support of telecommunications equipment described in this Category, are regarded as specially designed components, provided they are the standard models customarily supplied by the manufacturer. This includes operation, administration, maintenance, engineering or billing computer systems.*

1051. Equipment, Assemblies and Components

a. Any type of telecommunications equipment having any of the following characteristics, functions or features:

   1. Specially designed to withstand transitory electronic effects or electromagnetic pulse arising from a nuclear explosion;
   2. Specially hardened to withstand gamma, neutron or ion radiation;
   3. Specially designed to operate outside the temperature range from 218 K (-55°C) to 397 K (124°C);

   Notes:

   1. *1051.a.3. applies only to electronic equipment.*
   2. *1051.a.2. and 3. do not apply to equipment on board satellites.*

b. Telecommunication transmission equipment or systems, and specially designed components and accessories therefor, having any of the following characteristics, functions or features:

   Note:

   Telecommunication transmission equipment:

   a. Categorised as follows, or combinations thereof:

      1. *Radio equipment (e.g. transmitters, receivers and transceivers);*
      2. *Line terminating equipment;*
      3. *Intermediate amplifier equipment;*
      4. *Repeater equipment;*
      5. *Regenerator equipment;*
      6. *Translation encoders (transcoders);*
      7. *Multiplex equipment (statistical mutiplex included);*