D2.1 Spar On-board Modular Microcomputer

The architecture of the SPAR On-board Modular Microcomputer (SOMM) meets the key characteristics of advanced spacecraft computers outlined in section 1.1 and is the proposed computer for Paxsat missions.

The following description highlights the flexibility and expansion capability of SOMM.

D2.1.1 Configuration

SOMM can be configured from a pool of modules by switching secondary power rails to individual modules. A total of 16 prime modules connected to the unit bus may be powered at any given time.

D2.1.2 Unit Bus

A serial data communications bus (unit bus) interconnects modules within SOMM and supports bus access by priority arbitration, synchronous operation, shared resources, and multiprocessing capability.

The unit bus controller provides and conditions all unit bus signals, which are clock, sync, command data, reply data, real-time clock, reset, and bus select.

The transmission of 16-bit data words at a clock rate of 1 MHz yields a data rate of approximately 46K bytes/S.

D2.1.3 16-Bit CPU Module

The central processor of the 16-bit CPU module is the Texas Instruments SBP9989 operating at 3 MHz.

The 16-bit CPU memory contains up to 4K bytes of power-strobed PROM and 60K bytes of RAM.

Memory data error protection and correction (EDC) is achieved by means of PROM error detection (parity checking at the bit level) as well as RAM single error correction and double error detection (Hamming code).

Other features of the CPU module include real-time clock process control, priority interrupt handling, DMA, memory-mapped I/O, memory write protection, and process protection by a watch-dog timer.