Note Z:
In simple logic operations, a single instruction performs a single logic manipulation of no more than two operands of given lengths.
In complex logic operations, a single instruction performs multiple logic manipulations to produce one or more results from two or more operands.
Rates should be calculated for all supported operand lengths considering both pipelined operations (if supported), and non-pipelined operations using the fastest executing instruction for each operand length based on:

1. Pipelined or register-to-register operations. Exclude extraordinarily short execution times generated for operations on a predetermined operand or operands (for example, multiplication by 0 or 1.. If no register-to-register operations are implemented, continue with 2;
2. The faster of register-to-memory or memory-to-register operations; if these also do not exist, then continue with 3;
3. Memory-to-memory.

In each case above, use the shortest execution time certified by the manufacturer.

## Step 2: TP for each supported operand length WL:

Adjust the effective rate R (or $\mathrm{R}^{\prime}$ ) by the word length adjustment L as follows:

$$
\begin{aligned}
& \mathrm{TP}=\mathrm{R} * \mathrm{~L} \\
& \text { where } \mathrm{L}=(1 / 3+\mathrm{WL} / 96)
\end{aligned}
$$

## Note:

The word length WL used in these calculations is the operand length in bits. (If an operation uses operands of different lengths, select the largest word length.)
The combination of a mantissa ALU and an exponent ALU of a floating point processor or unit is considered to be one "CE" with a Word Length (WL) equal to the number of bits in the data representation (typically 32 or 64) for purposes of the "CTP" calculation.
This adjustment is not applied to specialised logic processors which do not use XOR instructions. In this case TP $=R$.
Select the maximum resulting value of TP for:
Each XP-only "CE" ( $R_{x p}$ );
Each FP-only "CE" ( $R_{f p}$ );
Each combined FP and XP "CE" (R);
Each simple logic processor not implementing any of the specified arithmetic operations; and
Each special logic processor not using any of the specified arithmetic or logic operations.

## Step 3: "CTP" for aggregations of "CEs", including CPUs.

For a CPU with a single "CE",

$$
" \mathrm{CTP} "=\mathrm{TP}
$$

(for "CEs" performing both fixed and floating point operations $\left.\mathrm{TP}=\max \left(\mathrm{TP}_{\mathrm{fp}}, \mathrm{TP}_{\mathrm{xp}}\right)\right)$
"CTP" for aggregations of multiple "CEs" operating simultaneously is calculated as follows:

## Notes:

1. For aggregations that do not allow all of the "CEs" to run simultaneously, the possible combination of "CEs" that provides the largest "CTP" should be used. The TP of each contributing "CE" is to be calculated at its maximum value theoretically possible before the "CTP" of the combination is derived.

## N.B.:

To determine the possible combinations of simultaneously operating "CEs", generate an instruction sequence that initiates operations in multiple "CEs", beginning with the slowest "CE" (the one needing the largest number of cycles to complete its operation) and ending with the fastest "CE". At each cycle of the sequence, the combination of "CEs" that are in operation during that cycle is a possible combination. The instruction sequence must take into account all hardware and/or architectural constraints on overlapping operations.
2. A single integrated circuit chip or board assembly may contain multiple "CEs".
3. Simultaneous operations are assumed to exist when the computer manufacturer claims concurrent, parallel or simultaneous operation or execution in a manual or brochure for the computer.
4. "CTP" values are not to be aggregated for "CE" combinations (inter)connected by "Local Area Networks", Wide Area Networks, I/O shared connections/devices, 1/O controllers and any communication interconnection implemented by software.
5. "CTP" values must be aggregated for multiple "CEs" specially designed to enhance performance by aggregation, operating simultaneously and sharing memory,- or multiple memory/"CE"- combinations operating simultaneously utilizing specially designed hardware.
This aggregation does not apply to "electronic assemblies" described by 1041.3.c.
$" C T P^{\prime}=T P_{1}+C_{2}{ }^{*} T P_{2}+\ldots+C_{n}{ }^{*} T P_{n}$,
where the TPs are ordered by value, with TP 1 being the highest, TP 2 being the second highest, ..., and TP $n$ being the lowest. $\mathrm{C} i$ is a coefficient determined by the strength of the interconnection between "CEs", as follows:

For multiple "CEs" operating simultaneously and sharing memory:

$$
C_{2}=C_{3}=C_{4}=\ldots=C_{n}=0.75
$$

## Notes:

1. When the "CTP" calculated by the above method does not exceed 194 Mtops, the following formula may be used to calculate Ci:
$C i=\frac{0.75}{\sqrt{m}}(i=2, \ldots, n)$
where $m=$ the number of "CEs" or groups of "CEs" sharing access provided:
a. The TPi of each "CE" or group of "CEs" does not exceed 30 Mtops;
b. The "CEs" or groups of "CEs" share access to main memory (excluding cache memory) over a single channel; and
c. Only one "CE" or group of "CEs" can have use of the channel at any given time.
N.B.:

This does not apply to items controlled under Category 1030.
2. "CEs" share memory if they access a common segment of solid state memory. This memory may include cache memory, main memory or other internal memory. Peripheral memory devices such as disk drives, tape drives or RAM disks are not included.

For Multiple "CEs" or groups of "CEs" not sharing memory, interconnected by one or more data channels:

$$
\begin{aligned}
C i & =0.75 * k_{i}(i=2, \ldots, 32)(\text { see Note below }) \\
& =0.60 * k_{i}(i=33, \ldots, 64) \\
& =0.45 * k_{i}(i=65, \ldots, 256) \\
& =0.30 * k_{i}(i>256)
\end{aligned}
$$

The value of $\mathrm{C} i$ is based on the number of "Ces", not the number of nodes. where $\quad k_{i}=\min \left(S_{i} / K_{r}, 1\right)$, and
$K_{r}=$ normalizing factor of $20 \mathrm{MByte} / \mathrm{s}$.
$S_{i}=$ sum of the maximum data rates (in units of MByte/s) for all data channels connected to the $i^{\text {th }}$ "CE" or group of "CEs" sharing memory.

When calculating a $C_{i}$ for a group of "CEs", the number of the first "CE" in a group determines the proper limit for $C_{j}$. For example, in an aggregation of groups consisting of 3 "CEs" each, the 22nd group will contain "CE" 64 . "CE" 65 and "CE" 66 The proper limit for Ci for this group is 0.60 .

Aggregation (of "CEs" or groups of "CEs") should be from the fastest-toslowest; i.e.:
$T P_{1} \geq T P_{2} \geq \ldots \geq T P n$, and
in the case of $T P_{i}=T P_{i}+1$, from the largest to smallest; i.e., : $C_{i} \geq C_{i}+{ }_{1}$

## Note:

The ki factor is not to be applied to "CEs" 2 to 12 if the TPi of the "CE" or group of "CEs" is more than 50 Mtops; i.e., Ci for "CEs" 2 to 12 is 0.75.

