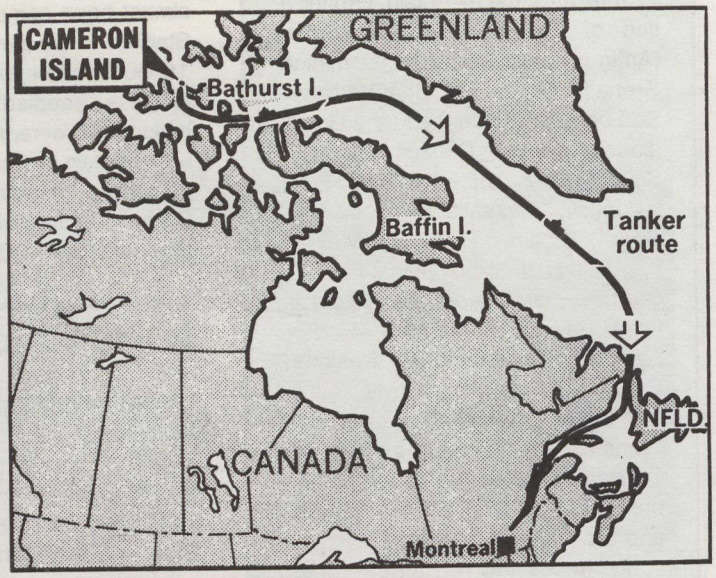
Historic oil shipment from the Canadian Arctic

The first commercial shipment of crude oil from the Canadian Arctic arrived at Petro-Canada's Montreal refinery on September 10. The shipment was made by Panarctic Oils Limited, a Calgary-based consortium of more than 30 Canadian oil exploration companies.

Energy, Mines and Resources Minister Pat Carney and Indian and Northern Affairs Minister David Crombie called the shipment a "milestone in Canadian history". Mr. Crombie added that "Panarctic's hard work and determination have proved that a Canadian company can exploit this country's rich resources in the far north for the benefit of present and future generations of Canadians".



The Globe and Mail

Route of the historic oil shipment from Arctic.

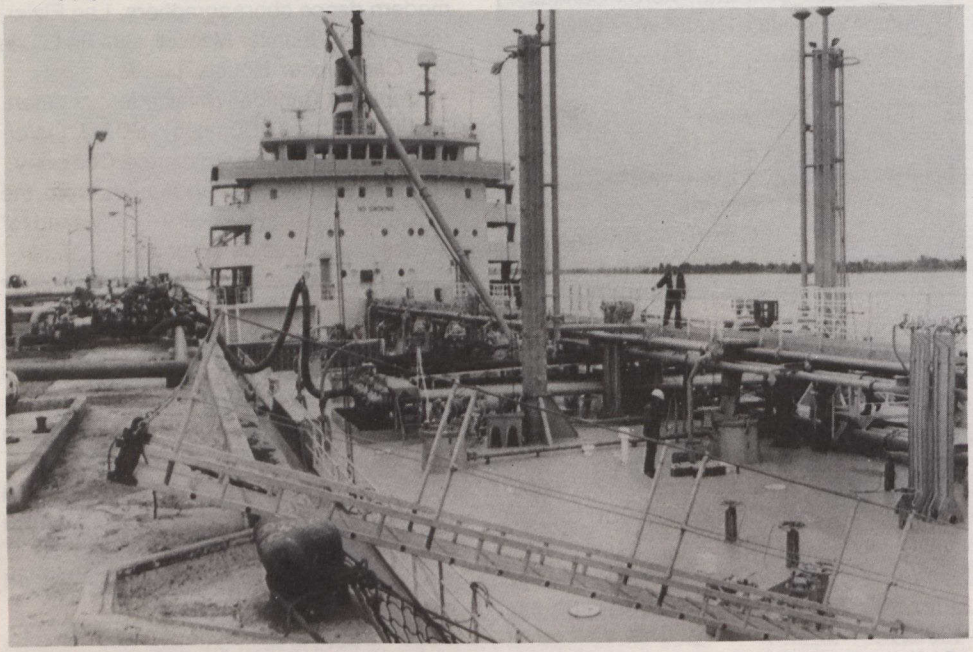
The 16 000 cubic metres of crude oil were shipped some 5 400 kilometres from Panarctic's Bent Horn oil field on Cameron Island in three weeks aboard the MV *Imperial Bedford.*

Commercially profitable

Panarctic hopes to ship enough of the light oil, used for such products as gasoline and heating oil, from the North in ten years to supply all the light oil Canada now imports, which is about one-third of total domestic oil consumption.

The consortium is expected to earn $1.5 million in profit on the first shipment and plans to move 16 000 cubic metres of crude next year and again in 1987. During the second phase of the project, due to begin in 1988, shipments are expected to increase to about 8 000 cubic metres a day.

Panarctic has operated 121 wells in the Arctic since 1968, out of a total drilling effort of 172 wells in the entire region. The Bent Horn field is estimated to contain between 56 million and 80 million cubic metres.


Canapress

The MV Imperial Bedford, *which transported the first commercial shipment of crude oil from the Canadian Arctic to Montreal – some 5 400 kilometres – in three weeks.*

Chip flaw detector

An engineering team led by Frank Shepherd, manager of the advanced technology laboratory at Bell Northern Research (BNR) Limited in Ottawa, has combined a scanning electron microscope (SEM) with a measuring technique called voltage contrast to detect flaws in new chip designs.

Using SEM technology to detect design flaws in integrated circuits could cut up to three months off the time it takes to get a new chip to market, said Cesar Cesaratto, vice-president of hardware technology development at BNR. Such savings may also lengthen the life cycle of a chip and result in greater revenue for a manufacturer, he added.

As new chip designs have become denser, smaller and faster, the SEM technique has become essential, Mr. Cesaratto said. Mechanical testing techniques require physical contact between the testing probe and the chip, which means that the chip can be more easily damaged and the techniques are less effective because of the smaller surfaces that need to be measured.

Voltage system developments

Advances in developing the voltage contrast system have been important in the development of SEM technology. While both the mechanical and SEM techniques measure voltage waveforms — the signals that go through a circuit — on conductors to determine if a chip is working correctly, the old system uses needle-like probes and the new system uses an electron beam within the SEM that can be positioned on smaller areas.

The best mechanical probe can only provide contact on conductors down to three micrometres (millionths of a metre) in diameter, and optical microscope images. A SEM can provide an image of points as small as five nanometres (billionths of a metre).

Using the SEM, designers get a highly magnified view of the part of the chip they want to investigate. The image appears on a monitor screen.

The voltage contrast equipment detects the voltage in the circuit and acts like a stroboscope, taking fast snapshots of the circuit. The designer traces the path of the current in high-speed intervals to determine if a signal is where it should be at all times. In this way, faults can be quickly detected.

BNR engineers are currently developing a more sophisticated testing station that could test many chips on silicon wafers. Such a station would allow further testing during the manufacturing process to determine which chips on a wafer are flawed.